

### R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

### SUPPORT FOR CLAIM AMENDMENT

Support for the amendments to the claims can be found in the drawings as originally filed, for example, FIG. 3 and in the specification as originally filed, for example, on page 21, line 3 through page 23, line 2, on page 26, line 3 through page 27, line 2, and on page 30, lines 12-15. As such, no new matter has been introduced.

### IN THE SPECIFICATION

The objection to the title is respectfully traversed and should be withdrawn. The Office Action provides no basis for the position taken that the current title is not descriptive (see page 2, lines 6-7 of the Office Action). The title is believed to be technically correct and descriptive of the invention claimed. As such, the objection should be withdrawn. However, if the objection is maintained, Applicants' representative respectfully requests that the Examiner provide reasons why the title is considered to be non-descriptive and a suggestion of a title that would be acceptable.

The specification has been amended for consistency to update the status of related cases.

#### CLAIM OBJECTIONS

The objection to claim 16 is respectfully traversed and should be withdrawn. The conclusory statement that the circuit claimed cannot be part of the Java virtual machine is not technically correct. One skilled in the art would understand the use of software necessarily involves a corresponding hardware platform. Specifically, the realization of a Java virtual machine implemented in software requires that the Java virtual machine software be run on a hardware platform. Furthermore, the specification provides that one technique for speeding up the execution of Java instructions is a full hardware implementation of the Java virtual machine such as a picoJAVA® core (see page 4, lines 7-13 of the specification). Furthermore, the specification states that FIG. 1 illustrates a Java virtual machine comprising a hardware portion 92 and a software portion 94. The Office Action fails to present any factual evidence establishing doubt as to the statements made in the specification. Therefore, the position taken in the Office Action on page 2, lines 11-15 that a Java virtual machine "is known as a software-based 'computer,' and is not a real computer, but exists only in software" and "the circuit claimed can not [sic] be part of the Java Virtual Machine" is not

technically correct. As such, the objection to claim 16 should be withdrawn.

**CLAIM REJECTIONS UNDER 35 U.S.C. §102**

The rejection of claims 1-6, 8, 9, 12-14 and 17-19 under 35 U.S.C. §102(b) as being anticipated by Hilgendorf et al. (U.S. Patent No. 5,925,124, hereinafter Hilgendorf) has been obviated by appropriate amendment and should be withdrawn.

Hilgendorf is directed to dynamic conversion between different instruction codes by recombination of instruction elements (Title).

In contrast, the present invention (claim 1) provides a circuit configured to translate instruction codes of a first instruction set on-the-fly into addresses into a microcode memory containing sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set. Claims 17 and 18 include similar limitations. Hilgendorf does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Hilgendorf appears silent regarding translating instruction codes on-the-fly, as presently claimed.

Specifically, Applicants' representative has downloaded an electronic version of the Hilgendorf reference and performed a search for the words "on the fly." No such occurrences were found.

Furthermore, Hilgendorf is silent about a microcode memory containing sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set, as presently claimed. In particular, Hilgendorf refers to **converting** microcode instructions of a code A B internal instructions of a code B, **not translating** instruction codes of a first instruction set on-the-fly **into addresses into a microcode memory containing sequences of instruction codes of a second instruction set** that emulate a functionality of the instruction codes of the first instruction set, as presently claimed. Specifically, Hilgendorf states:

There exist two possible methods for applying the instruction conversion mechanism described to microcode instructions. The first method is to relate each microcode instructions of code A to a huge number of explicitly defined internal instructions of code B. Of course, these internal instructions would have to be generated sequentially.

The second method is to first **translate said microcode instructions of code A** to the corresponding sequence of hard-wired instructions of code A. Then, in a next step, each of the hard-wired external instructions has to be translated to the corresponding sequence of internal instructions by means of the translation table 106. The advantage of this, second solution is that for each hard-wired external instruction, the corresponding internal instructions can be

generated in parallel (column 11, lines 53-67 of Hilgendorf, emphasis added).

Therefore, Hilgendorf does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, rather than **translating** instruction codes of a first instruction set on-the-fly **into addresses into a microcode memory** containing sequences of instruction codes of a second instruction set as presently claimed, Hilgendorf **converts** instructions of a code A (i.e., external instructions 100 of Hilgendorf) into instructions of a code B (i.e., internal instructions 101 or 400 of Hilgendorf) **by rearranging elements** of the instructions of the code A **using multiplexers** (see, for example, FIGS. 1 and 5 and abstract of Hilgendorf). Since Hilgendorf (i) is silent regarding a microcode memory containing sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set, as presently claimed and (ii) **converts** instructions of a code A into instructions of a code B **by rearranging elements** of the instructions of the code A using multiplexers, Hilgendorf does not disclose or suggest a circuit configured to **translate instruction** codes of a first instruction set on-the-fly **into addresses into a microcode memory** containing

sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set, as presently claimed. Therefore, Hilgendorf does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-16 and 19-20 depend, either directly or indirectly, from claims 1 or 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

**CLAIM REJECTIONS UNDER 35 U.S.C. §103**

The rejection of claims 7, 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Hilgendorf has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 10, 11 and 20 under 35 U.S.C. §103(a) as being unpatentable over Hilgendorf in view of Martin (U.S. Patent No. 4,439,828) has been obviated by appropriate amendment and should be withdrawn.

Claims 2-16 and 19-20 depend, either directly or indirectly, from claims 1 or 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be allowable.

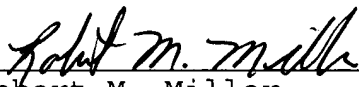
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

  
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Robert M. Miller  
Registration No. 42,892

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c/o  
LSI Logic Corporation  
1621 Barber Lane, M/S D-106 Legal  
Milpitas, CA 95035

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